BASIS OF ELECTROMAGNETIC COMPATIBILITY OF INTEGRATED CIRCUIT

Chapter IX - Standard measurement methods for IC susceptibility

Corrections of exercises

I. EXERCISE NO 1 - TEM cell vs. IC stripline

1. Compute the power delivered by an amplifier to induce 200, 400 and 800 V/m within the TEM cell presented in Fig. 8- 9.

2. The TEM cell is terminated by a 50 Ω load which withstands a maximum dissipation of 10 W. Is the dimensioning correct?

3. An IC stripline 50 mm wide is now considered. What should the distance separating the active conductor from the ground plane be to ensure a characteristic impedance of 50 Ω +/- 1 Ω?

4. What should the power delivered by a power amplifier to the IC stripline be to induce 800 V/m? Is the load defined in question 2 adequate to terminate the IC stripline?

Corrections:

1. If the TEM cell is perfectly matched to 50 Ω, the electric field at the center of the cell is given by:

$$E = \frac{\sqrt{P_{forw} \times 50}}{h}$$

where h is the septum height and P_{forw} is the forward power. In case of a perfect matching, the delivered power to the TEM cell loas is equal to the forward power. The delivered power is given by:

$$P_{forw} = \frac{E^2 h^2}{50}$$

The power values required to induce 200, 400 and 800 V/m are 1.6 W, 6.5 W and 25.9 W respectively.

2. According to the answers to the previous question, the load is correctly dimensioned for a maximum electric field of 400 V/m, but it will be damaged for a test at 800 V/m due to overheating.

3. According to equation 9-9, the separation distance should be equal to 10 mm.

4. As the active conductor of the IC stripline is 4.5 times closer to the IC under test than the TEM cell septum, the coupling with the IC under test is 20log(4.5) = 13 dB better in IC stripline than with the TEM cell. If both coupling devices are perfectly matched, with the same excitation power, the electric and magnetic fields will be 4.5 times or 13 dB larger in the IC stripline than in the TEM cell. Inversely, nearly 20 times (4.5^2) or 13 dB less power is required to produce the same electric or magnetic fields. Thus, to produce 800 V/m with the IC stripline, the power delivered by the amplifier is equal to: 25.9 / 20 = 1.3 W.

As the load defined in question 2 can withstand a maximum dissipation of 10 W, the load is correctly dimensioned. It will not be damaged during a susceptibility test in IC stripline.

II. EXERCISE NO 2 - BCI virtual test bench

The BCI probe presented in part 3.2 is considered in this exercise. The objective of the exercise is to determine the power required to inject a current of 200 mA in a cable harness during a BCI test, and then evaluate the susceptibility of an interface circuit (CAN bus transceiver – ISO 11898). The BCI test is performed in an open-loop configuration between 150 kHz and 400 MHz. During the BCI test, the power delivered by the amplifier cannot exceed 50 dBm. The model of the probe is given in file book\ch9\BCI_Model_HF.sch (Fig. 9- 7).

In order to determine the power required to inject a given current along a cable harness, the calibration set-up presented in part 3.3 is used. The BCI probe is connected to an RF amplifier and a bidirectional coupler to measure the forward power. The BCI probe is clamped around the jig, which is terminated by a 50 Ω load on one side, and a spectrum analyser on the other side to measure the induced current. The electrical model of coupling between the BCI probe and the calibration jig is given in file Clamp_coupling_calib_jig.sch (Fig. 9- 9).

1. Build an electrical model of the calibration of the BCI probe on the jig. Place the bidirectional coupler symbol  to extract the forward power, and a current probe to measure the induced current on the jig.

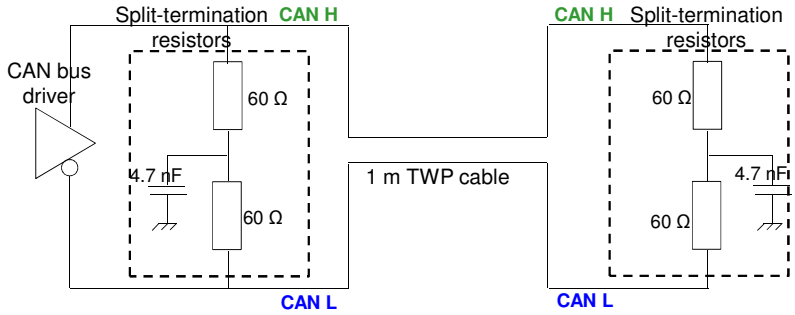
2. With the previous electrical model, determine the forward power required to induce 200 mA in the calibration jig. Fill in the following table.

Frequency	RF generator voltage (V)	Forward power required to induce 200 mA (dBm)	Max. forward power during BCI test (dBm)
150 kHz			
300 kHz			
1 MHz			
3 MHz			
10 MHz			
30 MHz			

100 MHz			
400 MHz			

3. The BCI test is performed on a CAN bus driver dedicated to automobile applications. The driver is compatible with the specifications of ISO standard 11898-2 (high-speed CAN, data rate up to 1 Mbits/s). The CAN bus is a differential bus (impedance of 120 Ω +/- 10 Ω) formed by two complementary signals: CANH and CANL. The electrical characteristics with which the differential signal must comply are given in the table below. The bus structure is presented in the figure below. The driver is connected to a one-metre-long twisted-wire pair (TWP) cable terminated by split-termination resistors at each end. The cable is routed 5 cm above a reference ground plane. During the BCI test, the BCI probe is clamped around both wires of the TWP cable.

Logical level '0' (dominant level)	Differential voltage range: 0 to 0.5 V
Logical level '1' (recessive level)	Differential voltage range: 0.9 to 2 V
Common-voltage range	-7V to +12 V

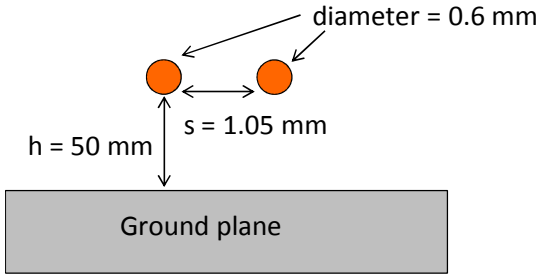


a. What is the nature of the current induced in the TWP cable?

b. What is the purpose of the 4.7 nF capacitor in the split-termination resistor? Is it a suitable value?

c. During the susceptibility test, the voltages induced at each end of the cable are measured. Propose two susceptibility criteria concerning the termination voltages.

4. The following figure describes the TWP cable cross-section. With the IC-EMC tool in "Tools > Cable modelling", compute the cable's odd and even characteristic impedances. Why is the cable suitable for a CAN bus application? Build an electrical model of the cable valid up to 400 MHz.



5. Construct the electrical model of the BCI on the CAN bus. The CAN driver is not modelled; only the split-termination resistors are considered. By default, the BCI probe is placed at the centre of

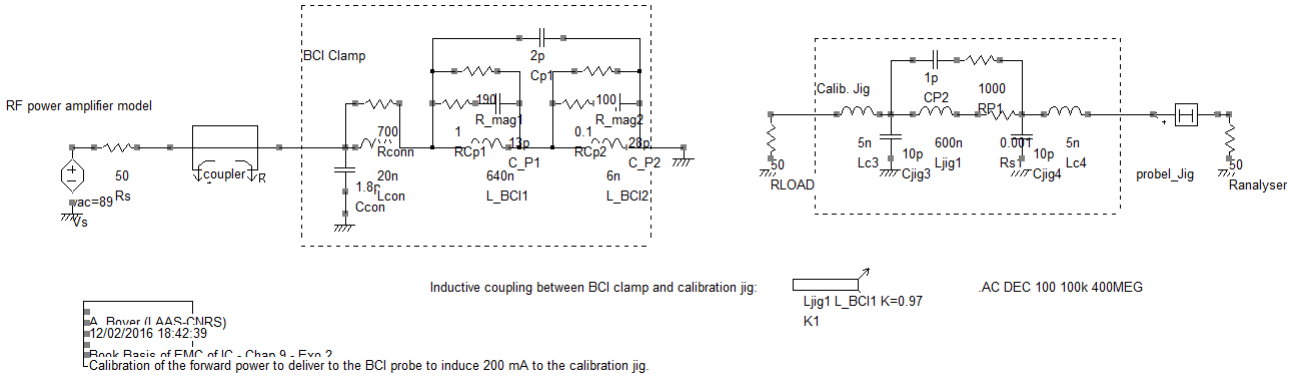
the cable. The magnetic coupling between the BCI probe and each wire of the cable is assumed to be identical to the magnetic coupling with the calibration jig.

6. For the frequencies listed in the table of question 2, simulate the differential- and common-mode voltages induced at each terminal. Comment on the results.

7. Termination resistor values are given with a tolerance of +/- 5 Ω. What is the effect of a mismatched termination resistor on the differential- and common-mode voltages induced at each terminal? Propose a general rule to improve the immunity of a differential bus to common-mode disturbance.

Corrections:

1. The electrical model of the calibration of the BCI probe can be found in the file BCI_Probe_Calib_jig.sch. The schematic diagram includes the model of the RF power amplifier and its coupler (in the left), the BCI clamp (in the middle) and the calibration jig (in the right) terminated by 50 Ω load at both extremities. The magnetic coupling between the BCI clamp and the jig is represented by the mutual coupling coefficient K1. A current probe is inserted between one terminal of the jig and the equivalent resistance of the measurement receiver. It aims at measuring the current induced along the jig.



2. With the model BCI_Probe_Calib_jig.sch, for each frequency, change the AC magnitude of the voltage source Vs until the current in the jig (monitored by the current probe probeI_Jig) reaches 200 mA. Measure also the forward power given by the bidirectional coupler to verify that it does not exceed the 50 dBm (100 W) limit.

The column 'RF generator voltage' is the AC amplitude of the voltage generator Vs when a current of 200 mA is induced in the jig. This voltage generator models the internal voltage of the power amplifier. The column 'Forward power required to induce 200 mA' gives the forward power when a current of 200 mA is induced in the jig. In practice, the forward power cannot exceed 50 dBm because of the power amplifier limits. If the required forward power exceeds the limits, the maximum power used during the test will be 50 dBm. The last column gives the practical maximum forward power used during the susceptibility test. If the forward power required to induce 200 mA is less than 50 dBm, this value is written in the last column. Otherwise, it is 50 dBm. Actually, it is not possible to induce 200 mA between 150 kHz and nearly 1 MHz.

Frequency	RF generator voltage (V)	Forward power required to induce 200 mA (dBm)	Max. forward power during BCI test (dBm)
150 kHz	1750	71.8	50
300 kHz	875	65.8	50
1 MHz	270	55.6	50
3 MHz	95	46.5	46.5
10 MHz	45	40	40
30 MHz	37	38.3	38.3
100 MHz	36	38.1	38.1
400 MHz	89	46	46

3. a. When a current circulates on the BCI probe, a voltage is induced by inductive coupling on every wires of the cable harness around which the BCI probe is clamped. Thus, it is common-mode voltage and common-mode current is induced on the cable harness.

3. b. The signal is transmitted along the CAN bus in differential mode. The CAN bus must have a differential characteristic impedance of 120 Ω. So the split-termination resistors aim at matching the ends of the CAN bus. The two 60 Ω resistors ensure a 120 Ω termination for the differential mode.

Ideally (if both 60 Ω resistors are identical), the 4.7 nF has no influence on the differential signal. But it has an influence on high-frequency common-mode signals that propagate on the cable, for example those induced by the BCI clamp. It filters the high-frequency common-mode signals by ensuring a low impedance path to the ground plane. Without this capacitor, the common-mode impedance is due to the parasitic capacitance between the cable, the CAN driver and receiver to the ground, which could be an uncontrolled and large impedance. It could lead to excessive common-mode voltage at bus terminals.

However, according to the electrical characteristics, a common-mode voltage must exist for a correct operation of the CAN bus (CANH and CANL voltages are usually between 1.5 and 3.5 V). Let call it the low-frequency common-mode voltage, whose bandwidth is nearly equal to 1 MHz. This filtering capacitor must not affect the nominal operation of the CAN bus, by filtering the low frequency common-mode voltage.The 60 Ω termination resistors and the filtering capacitor form a high-pass filter, whose cut-off frequency is equal to $1/\left(2\pi\frac{R}{2}C\right)=1.13\ MHz$ with C = 4.7 nF.

A larger capacitance value would reduce the cut-off frequency and affect the nominal operation of the CAN bus. Inversely a smaller capacitance would increase the cut-off frequency and would not filter enough the high frequency common-mode currents induced on the CAN bus.

3. c. According to the CAN bus characteristics, a proper operation is ensured if two conditions are met:

- the common-mode voltage remains in the range -7 V to 12 V.
- the differential-voltage remains in the range 0 - 0.5 V when a logical '0' is transmitted and in the range 0.9 - 2 V when a logical '1' is transmitted.

We suppose that the CAN bus driver operation is nominal without injection of high frequency disturbance. We can define two susceptibility criteria: the first one on the common-mode voltage induced by the BCI injection, the second one on the differential voltage due to the conversion of the common-mode to differential-mode currents.

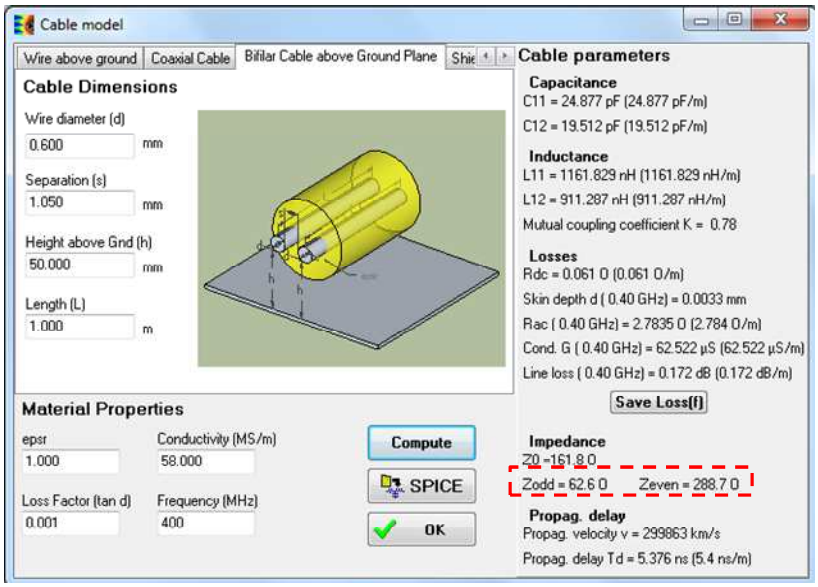
Susceptibility criterion 1: common-mode voltage

If we suppose that the nominal common-mode voltage is 0 V, the common-mode voltage induced by the BCI injection must not exceed 7 V.

Susceptibility criterion 2: differential-mode voltage

As the bit are encoded by the differential voltage between CANH and CANL, any differential-mode disturbance can add to the nominal differential signal and may lead to transmission errors due to bit misinterpretation. If a logical '0' is transmitted and if the nominal differential voltage is 0.5 V, a bit misinterpretation may arise if the differential-mode voltage induced by the BCI injection exceed 0.9-0.5 = 0.4 V. The situation is the same if a logical '1' is transmitted and if the nominal differential voltage is 0.9 V.

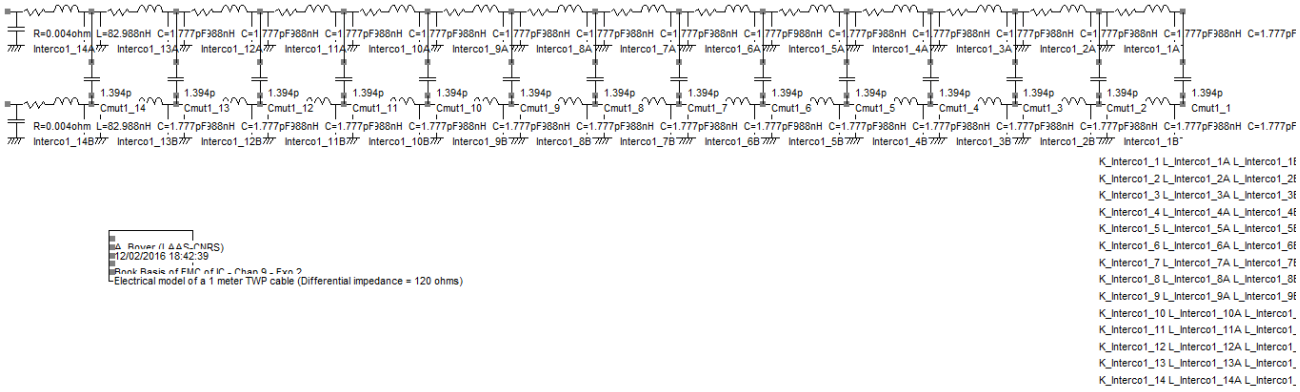
4. The tool 'Cable modeling' computes the p.u.l parameters, the characteristic impedance, the propagation delay of various types of transmission line. Select the line 'Bifilar Cable above Ground Plane', enter the line geometrical dimensions and click on the button 'Compute'. The characteristics of the line are given below:



The TWP cable above the ground plane is a three conductor transmission line on which two propagation modes coe-exist: even and odd modes. The line is characterized by an odd-mode characteristic impedance Zodd = 62.6 Ω and an odd-mode characteristic impedance Zeven = 288.7 Ω. The propagation along this line can also be expressed in differential and common-modes. The differential-mode characteristic impedance Zdiff = 2*Zodd = 125.2 Ω and Zcommon = Zeven/2 = 144.3 Ω.

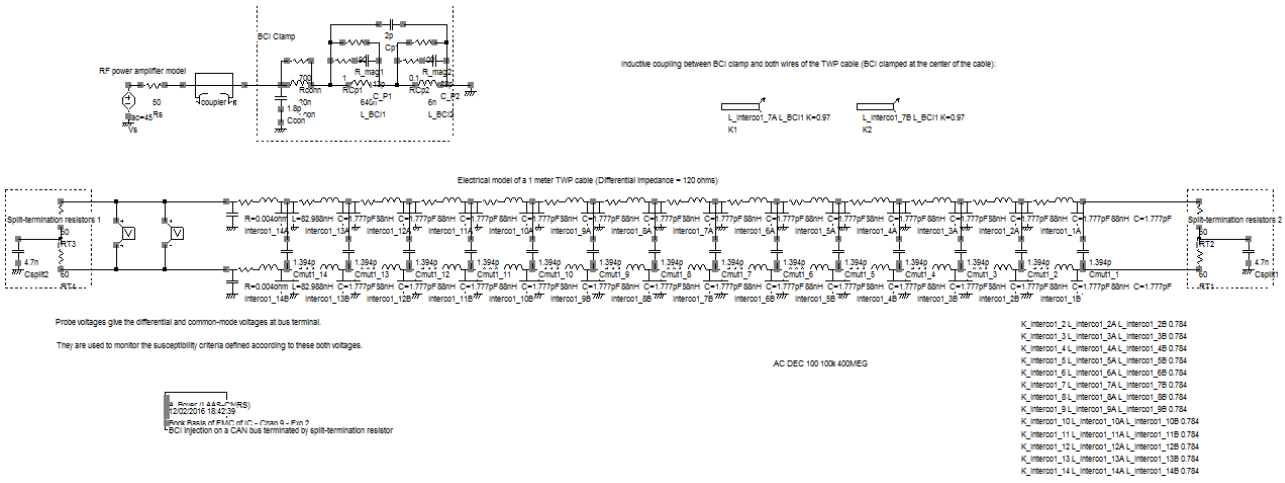
The ISO11898-2 specification requires cables with differential-mode characteristic impedance equal to 120 Ω +/- 10 Ω. This TWP cable satisfies this constraint.

Enter '400' in the filed 'Frequency (MHz)' and click on the button 'SPICE' to generate a RLC lumped model of the line. The model is formed by 14 RLC cells and is valid up to 400 MHz. Each cell models a 7.1 cm long section of the line. The model of the line is given in the file TWP_cable.sch.



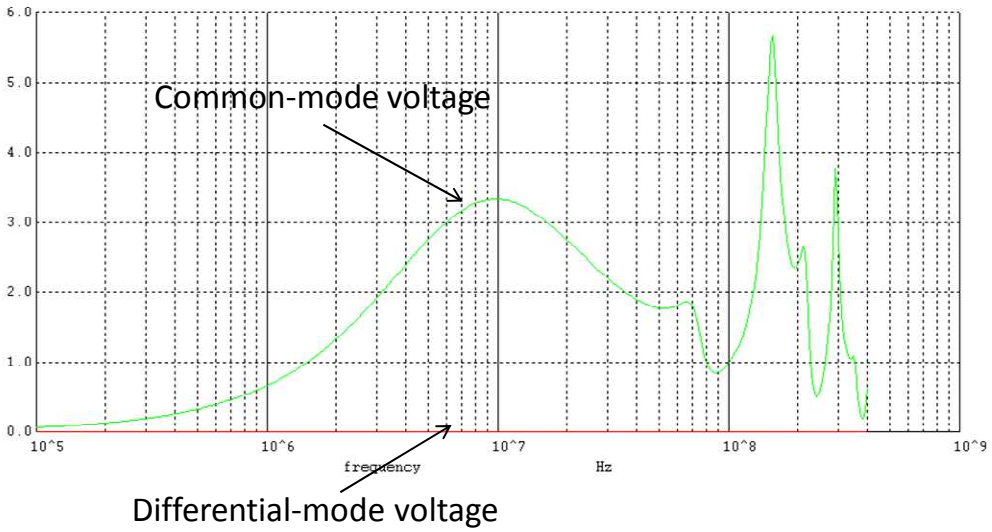
5. The electrical model of the BCI injection on the TWP cable terminated by split-termination resistors can be found in the file BCI_injection_CAN_bus.sch.The model includes:

- the model of the 1 m TWP cable constructed in the previous questions
- the split-termination resistors placed at each end of the cable
- the model of the power amplifier and the bidirectional coupler
- the model of the BCI probe
- two coupling coefficient K, which model the inductive coupling between the BCI probe inductance (L_BCI1) and a short section of both wires of the cable. As the probe is clamped at the center of the cable, the BCI probe inductance is coupled to the inductances L_Interco1_7A and L_Interco1_7B. Changing these inductances change the position of the BCI probe along the cable. The coupling coefficients are set to 0.97.
- a common-mode voltage probe  to monitor the common-mode voltage induced on one end of the cable
- a differential-mode voltage probe  to monitor the differential-mode voltage induced on one end of the cable



6. For each frequency, the AC magnitude of the voltage source Vs (the power amplifier) is set to the voltage found in the second column of the table of question 2. With these voltages, a current of 200 mA would be induced on the calibration jig. Actually, it does not guarantee the current induced on the TWP cable. A closed-loop configuration with a current monitoring probe should be used to verify the current induced on the cable.

For example, the graph below shows the simulation result when the AC magnitude of the voltage source Vs is set to 45 V (at 10 MHz, a current of 200 mA is induced on the jig). The common-mode voltage induced at 10 MHz is equal to 3.3 V while the differential-mode voltage is null. The evolution of the common-mode voltage according to the frequency is quite complex. It shows several maximum and minimum, related to the inductive coupling, BCI probe model, BCI probe position along the cable, cable characteristics (common-mode and differential impedances), cable terminations.



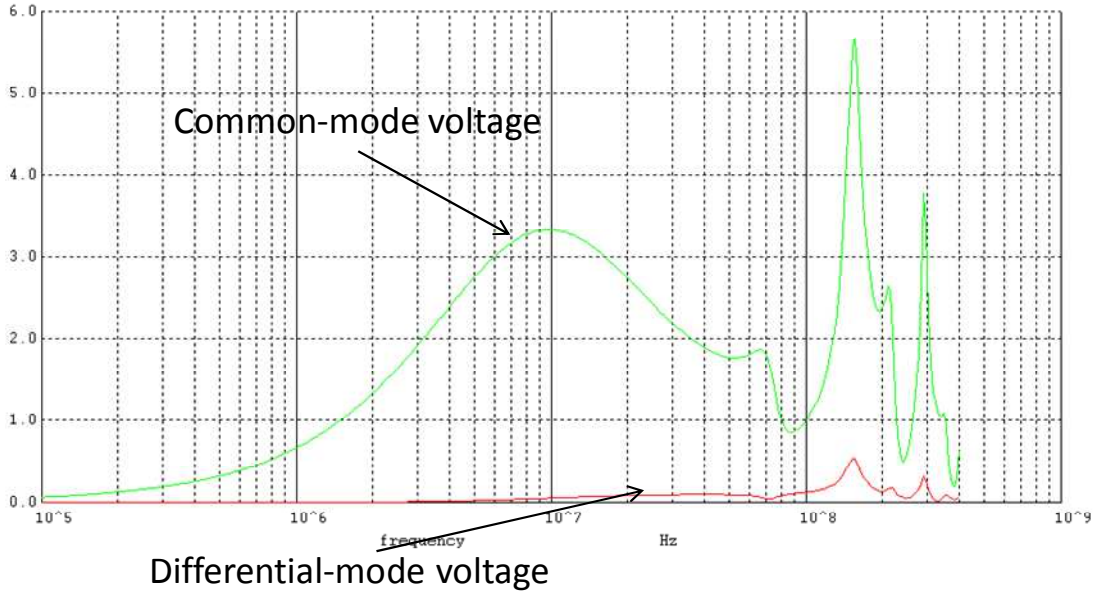
This simulation is repeated for each frequency of the table of question 2, with the AC magnitude of voltage source Vs to induce 200 mA on the calibration jig. The following table summarizes the results (RF generator voltages between 150 kHz and 1 MHz have been updated to ensure a forward power equal to 50 dBm.

Frequency	RF generator voltage (V)	Common-mode voltage (V)	Differential-mode voltage (V)
150 kHz	140	0.295	0
300 kHz	140	0.6	0
1 MHz	140	2.06	0
3 MHz	95	4.07	0
10 MHz	45	3.33	0
30 MHz	37	1.8	0
100 MHz	36	0.8	0
400 MHz	89	1.52	0

The induced common-mode voltage amplitude does not exceed 7 V. The differential-mode voltage is null whatever the frequency because of the perfect symmetry of the model:

- the inductive couplings between the BCI injection probe and both wires of the cable are identical, so there is no differential-mode injection
- the line is supposed perfectly symmetrical and the termination resistors are identical, so there is no conversion from common-mode to differential-mode disturbance.

7. The previous electrical model is transformed to take into account the variability in termination resistance values. The model can be found in the file BCI_injection_CAN_bus_mismatch.sch. For example, termination resistors take the value 63 and 57 Ω. For example, the graph below shows the simulation result when the AC magnitude of the voltage source Vs is set to 45 V. The common-mode voltage evolution with frequency is nearly unchanged. However, differential-mode voltage appears.



The following table summarizes the simulated common and differential mode voltages.

Frequency	RF generator voltage (V)	Common-mode voltage (V)	Differential-mode voltage (V)
150 kHz	140	0.295	10 µV
300 kHz	140	0.6	75 µV
1 MHz	140	2.06	0.002
3 MHz	95	4.07	0.018
10 MHz	45	3.33	0.053
30 MHz	37	1.8	0.076
100 MHz	36	0.8	0.099
400 MHz	89	1.52	0.156

The induced differential-mode voltage does not exceed 400 mV. The differential-mode voltage appears because the symmetry of the model is lost. Actually, any dissymetry brought by the terminations, by the CAN bus driver or receiver, cable or BCI probe injection may lead to differential-mode disturbance generation and common-mode to differential-mode conversion.

Differential-buses are not sensitive to common-mode disturbances, except if:

- the induced common-mode voltage exceeds a certain limit (the interface circuit may saturate or damage)
- there is a conversion of the common-mode noise into differential-mode noise due to dissymetry.

In the first case, a low impedance path for the common-mode has to be ensured to filter the common-mode voltage.

A general rule to improve differential-bus immunity is: ensure symmetry of the bus as much as possible to cancel common-mode to differential-mode conversion.

III. EXERCISE NO 3 - SilentCore EMC test plan

The SilentCore microcontroller is dedicated to high-reliability applications requiring very low electromagnetic noise. The circuit includes a 32-bit microprocessing unit. An on-chip PLL provides an internal operating clock running at 266 MHz from an external 16 MHz crystal oscillator. The microcontroller includes 1 MByte of SRAM and Flash memories and several peripherals: three general purpose I/O ports (ports A, B and C), four 12-bit ADC inputs, and a CAN bus controller. The following table provides the circuit's pin list.

The circuit has to pass tests to prove its low emission and high immunity. Propose an EMC test plan to qualify the circuit. For reasons of cost, the number of measurements has to be minimised. Detail the types of measurement, the tested pin and the injection level required for the susceptibility test.

Pin name	**Description**
VDD	Power supply
VSS	Ground
VDD_OSC	Oscillator power supply
VSS_OSC	Oscillator ground
PA[0..7]	Data port A (programmable drive)
PB[0..7]	Data port B (programmable drive)
PC[0..7]	Data port C (programmable drive) external 133MHz data/address
ADC In[0..3]	4 analogue inputs (12-bit resolution)
CAN Tx	CAN transmitting pin

CAN Rx	CAN receiving pin
XTL_1, XTL_2	Quartz oscillator 16MHz
CAPA	PLL external capacitance
RESET	Reset microcontroller

Corrections

The SilentCore circuit is a synchronous digital circuit, with a relatively large core (it is a 32-bit microcontroller) and several I/O ports, whose one is high speed (port C). This circuit may produce significant conducted and radiated emission. Since it is dedicated for applications which require low electromagnetic noise, the manufacturer has to verify that the parasitic emission from the SilentCore is small enough (this is one of the feature highlighted by the manufacturer).

The operation of microcontroller can be corrupted by electromagnetic disturbance. Moreover, electromagnetic disturbance may disturb the operation of several peripherals of the microcontroller (e.g. the on-chip PLL and the analog-to-digital converter). The manufacturer has to ensure that the robustness of the SilentCore is high enough for safety critical applications.

That's why the manufacturer has to perform both emission and susceptibility tests on this circuit, for example based on the standards IEC61967 and IEC62132 dedicated to emission and susceptibility measurements of ICs.

The objective of this exercise is to define the test plan, i.e. measurements that should be done to characterize emission and susceptibility of this circuit: the type of measurements, the list of tested pins, the configuration of the circuit, the frequency range, the maximum amplitude of disturbance for susceptibility tests, the test equipments …

Because of the duration and costs of EMC tests, it is important to optimize the number of tests without compromizing the precision of the test plan.

A special test board should be developed to conduct all the EMC tests. For example, the 100 x 100 mm multi-layer board proposed by IEC61967 standard is adapted for this type of tests (refer to chapter 6 part 5.1 for more details).

1. Test plan for measurements of electromagnetic emission

Conducted and radiated emission tests have to be performed, according to IEC61967 standard. The standard suggests to measure emission over the range 150 kHz up to 1 GHz. However, it is recommended to extend the frequency range if the circuit under test produces significant emission beyond this range.

An important concern is the configuration of the circuit during the emission tests. The following recommandations may be followed to select the circuit configurations and on-chip program:

- the configuration activates the circuit parts which contribute to emission. The different parts can be activated individually (to characterize the contribution of this part to the overall emission) or simultaneously. The first strategy is interesting for investigation purpose but it increases the number of tests.

- the configuration should be typical of a nominal operation. It can be defined with application designers
- The required equipments are spectrum analyser or EMI receiver, 50 Ω cables and preamplifier if necessary (especially for radiated emission test). Configurations of measurement equipments are provided by IEC61967 standard.

A. Radiated emission tests

IEC61967 proposes to test radiated emission in TEM (up to nearly 1 GHz) or GTEM cell (up to 10-18 GHz depending on the model). If the circuit under test is mounted on a test board such as the one proposed in IEC61967, the global radiated emission produced by the circuit can be characterized. The radiated emission of the circuit with different on-chip configurations can be tested to measure the contribution of the different parts of the circuit. As explained in chapter VIII part 3.3, the measurement results depend on the circuit orientation within the TEM cell. It is recommended to repeat measurements with the four possible orientations of the circuit to ensure that the worst-case emission is not missed.

Limits presented in Fig. 8-13 may be used. As the circuit is dedicated to applications requiring very low electromagnetic noise, class III limit should be considered.

B. Conducted emission tests

The standard IEC61967-4 proposes two methods for characterization of conducted emission: 1 Ω and 150 Ω probe.

Two 1 Ω probes should be placed:

- one on the Vss pin to characterize emission produced by the digital cores and I/O, which are the main contributors of conducted emission along power supply.
- the other on the VSS_OSC pin to characterize the conducted emission produced by the on-chip oscillator and PLL. Another advantage of this measurement is to verify the isolation of the on-chip oscillator and PLL from the noise produced by the other noisy parts of the circuit

Limits presented in Fig. 8-5 may be used. If the power supply is delivered by a voltage regulator mounted in close proximity of the microcontroller, the pins can be considered as local. As the circuit is dedicated to applications requiring very low electromagnetic noise, class III limit should be considered.

150 Ω probe should be placed to characterize conducted emission produced by output drivers. It is not necessary to test all the I/O pins, but all the driver types. For example, ports A and B contain the same type of I/O drivers, with the same options (e.g. reduced and full drive, slew rate). A 150 Ω probe can be connected to one pin of port A or B. This pin should be programmed the largest drive and slew rate modes for the test. Port C is different since I/O are designed for external memory interfacing. An additional 150 Ω probe should be connected to one pin of port C. CAN_TX produces also conducted emission and a 150 Ω probe should be connected on this pin.

Other pins are not tested since they do not produce conducted emission (they do not switch).

Limits presented in Fig. 8-5 may be used. If long traces may be connected to an output driver, the pin should be considered as global. As with limits of 1 Ω measurement, class III limits may be used.

2. Test plan for measurements of susceptibility

Conducted and radiated susceptibility tests have to be performed, according to IEC62132 standard. The standard suggests to measure emission over the range 150 kHz up to 1 GHz. If possible, it is recommended to extend the frequency range to verify that the circuit is not vulnerable at larger frequency.

An important concern is the definition of susceptibility criteria. The following recommendations can be followed to define them:

- the microcontroller embeds sensitive hardware peripherals such as oscillator, analog-to-digital converter, on-chip regulators, RF transceiver… The operation of these functions should be monitored
- if the microcontroller embeds critical-safety functions, their integrity should be tested (e.g. execution of a program, reading/writing of a memory)
- interface connected to long traces, cable harness, antenna are exposed to electromagnetic disturbances, so that their immunity should be tested
- if the circuit is dedicated to specific applications, the circuit configuration for susceptibility tests should be defined with application designers.

The circuit configuration and embedded programs are defined to monitor the susceptibility criteria during the susceptibility test.

The required equipments are RF synthesizer, power amplifier, bidirectional coupler, 50 Ω cables to generate the RF disturbances and couple them to the circuit. Equipments to monitor the circuit under test and detect failures have to be added. Power requirement of power amplifier is chosen according to the maximum amplitude of disturbance applied on the circuit under test.

A. Radiated susceptibility tests

IEC62132 proposes to test radiated susceptibility in TEM (up to nearly 1 GHz) or GTEM cell (up to 10-18 GHz depending on the model). If the circuit under test is mounted on a test board such as the one proposed in IEC61967, the global radiated susceptibility of the circuit can be characterized. The radiated susceptibility of the circuit with different on-chip configurations can be tested to measure the sensitivity of the different parts of the circuit to electromagnetic disturbance. As explained in chapter VIII part 3.3, the measurement results depend on the circuit orientation within the TEM cell. It is recommended to repeat measurements with the four possible orientations of the circuit to ensure that the worst-case susceptibility is not missed.

Maximum level defined in Table 9-3 can be used to test radiated susceptibility of the circuit. As the circuit is dedicated for high reliability application, the test severity should be level III (800 V/m). With the TEM cell model presented in Fig. 8-9, the power delivered by the amplifier should be larger than: $P_{\max} = \frac{(E \times h)^2}{50} = 26\,W$.

B. Conducted susceptibility tests

The standard IEC62132-4 proposes he Direct Power Injection (DPI) method to characterize the conducted susceptibility of IC pin. The following pins should be tested, with the maximum injected power level according to Table 9-1:

Pins	Justification	Maximum injection level
VDD	The digital core operation and I/O signal integrity depend on power supply voltage fluctuations	Class 2 (20 dBm)
VDD_OSC	The on-chip oscillator and PLL operation depends on the power supply integrity	Class 2 (20 dBm)
One pin of PortA or B	Susceptibility of digital input buffer to incoming conducted disturbance. Only one pin is tested since both ports include the same type of buffer.	Class 2 or 3 (10-20 dBm) depending on the length of traces connected to these pins
One pin of PortC	Susceptibility of digital input buffer to incoming conducted disturbance. Only one pin is tested since both ports include the same type of buffer.	Class 2 or 3 (10-20 dBm) depending on the length of traces connected to these pins
ADC_IN	Susceptibility of analog input buffer to incoming conducted disturbance. Only one pin is tested since the four analog inputs are identical.	Class 2 or 3 (10-20 dBm) depending on the length of traces connected to these pins
CAN_RX, CAN_TX	Susceptibility of transmitting and receiving digital pins of CAN transceiver. Both pins have to be tested	Class 2 or 3 (10-20 dBm) depending on the length of traces connected to these pins
CAPA	Disturbance coupled to this pin can affect PLL operation.	Class 3 (10 dBm) since this pin is local
XTL1, XTL2	Disturbance coupled to this pin can affect oscillator operation.	Class 3 (10 dBm) since this pin is local
RESET	Excessive disturbance coupled to this pin can trigger unwanted circuit reset	Class 3 (10 dBm) since this pin is local